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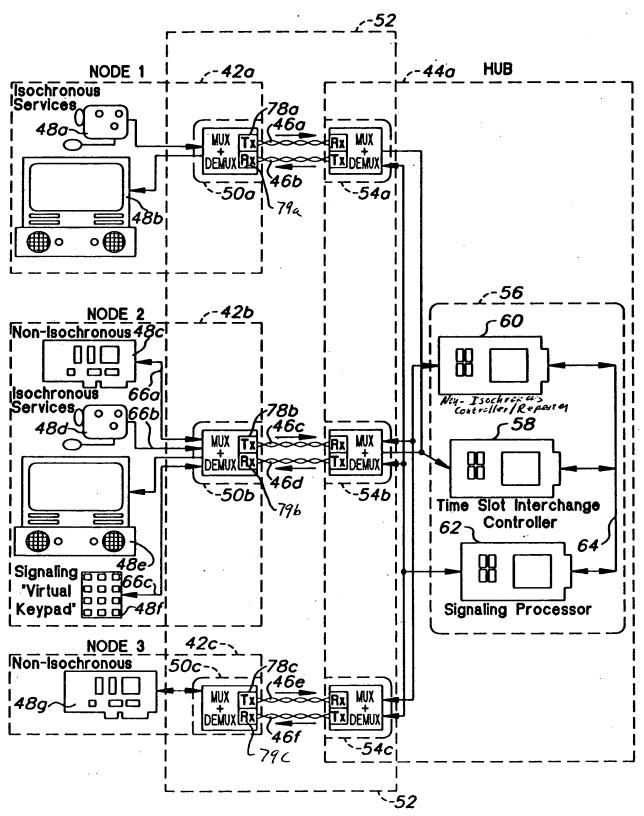


Fig 2

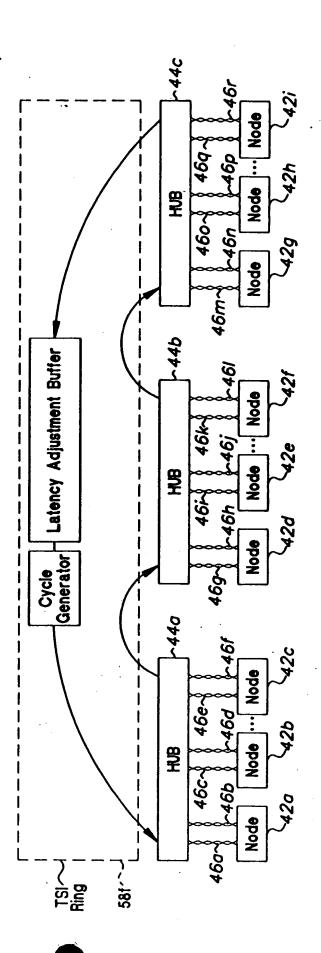


Fig 3A

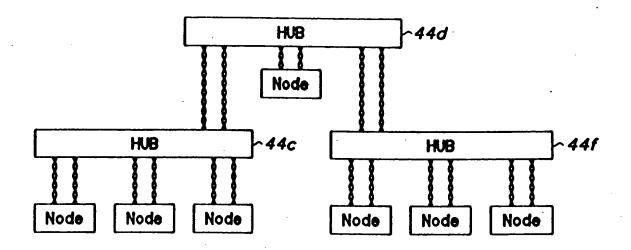


Fig 3B

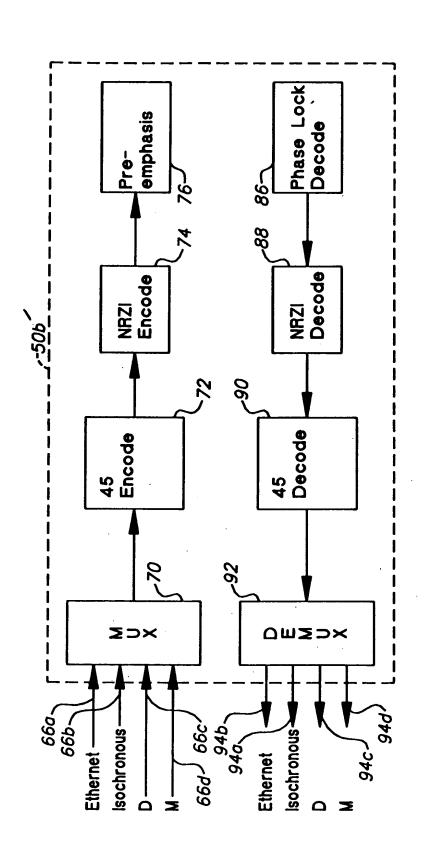
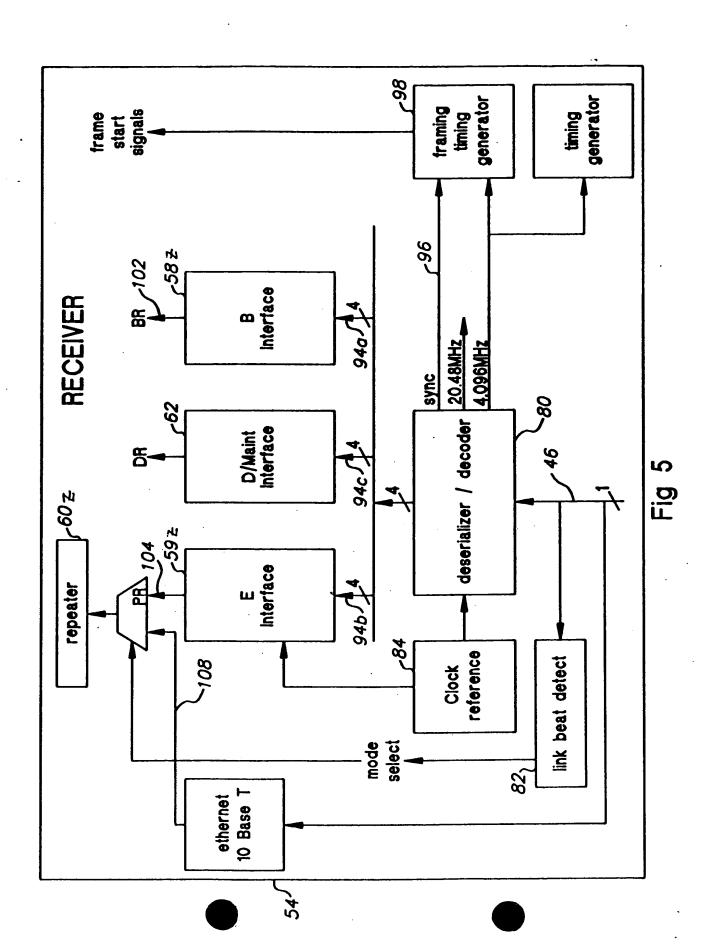
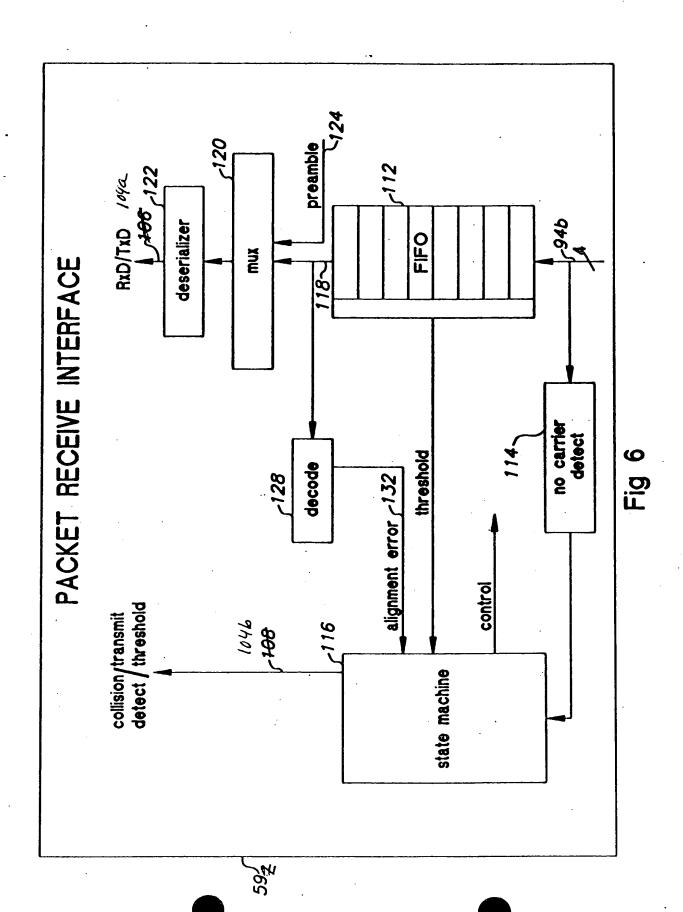
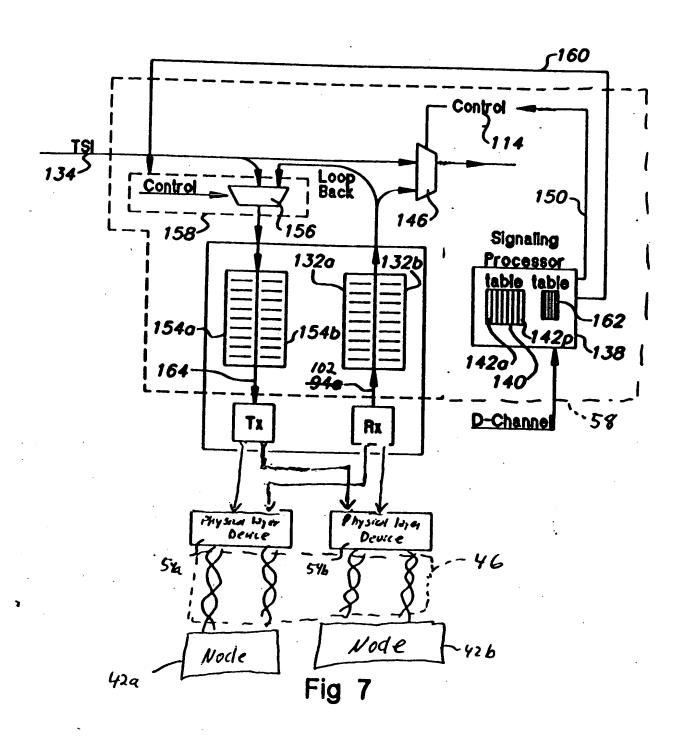


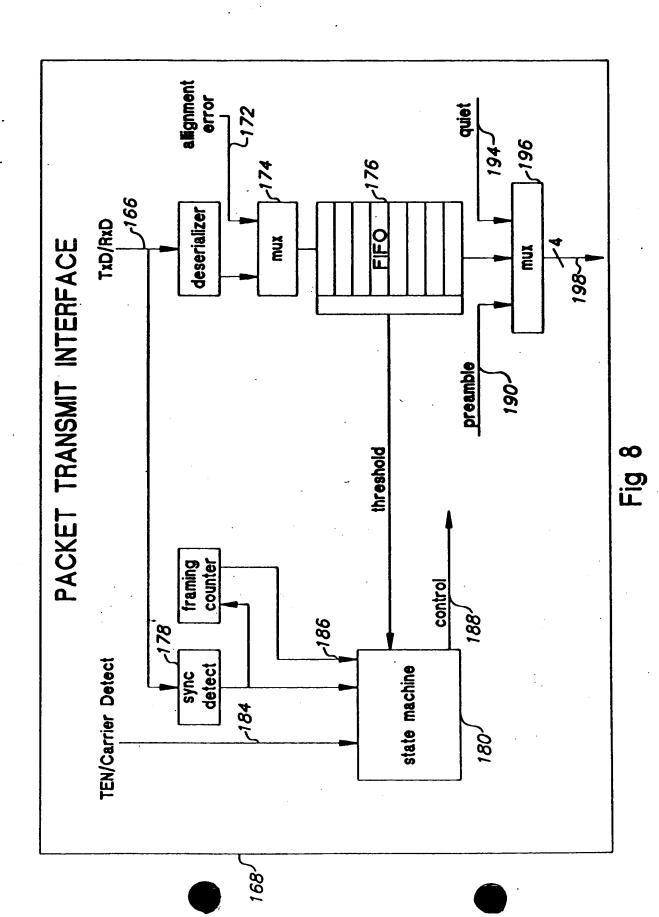
Fig 4

12%









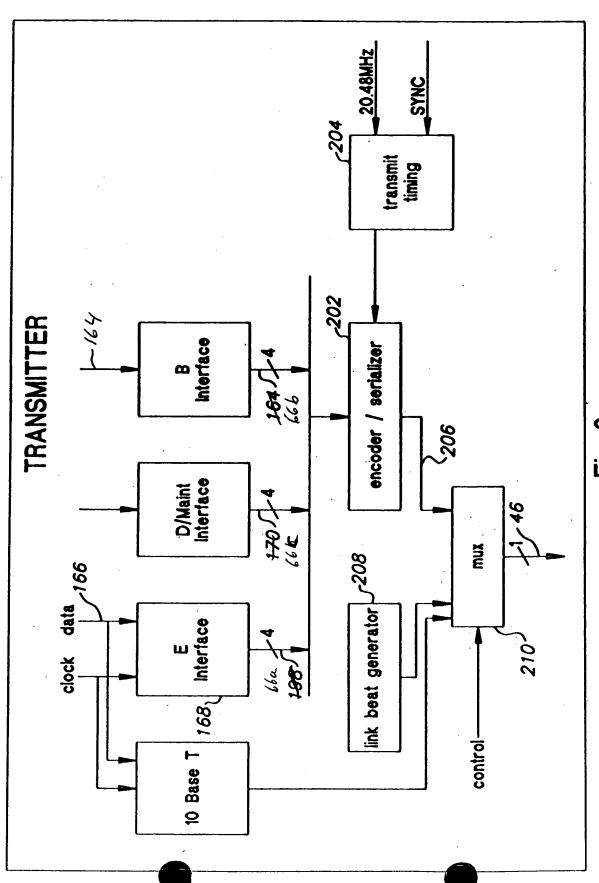


Fig 9

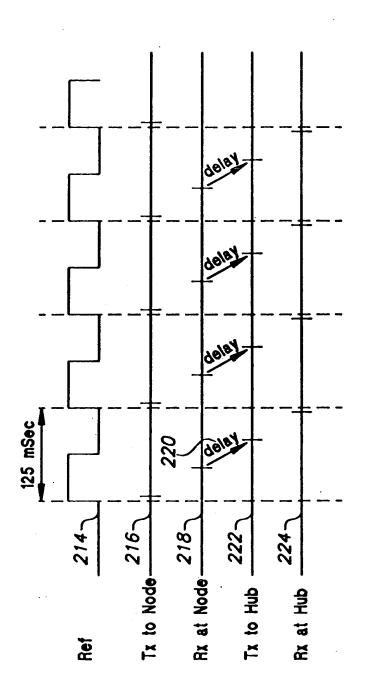


Fig 10

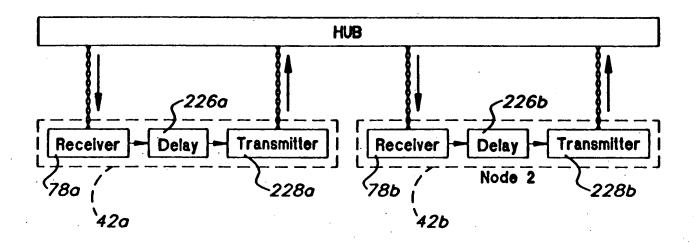
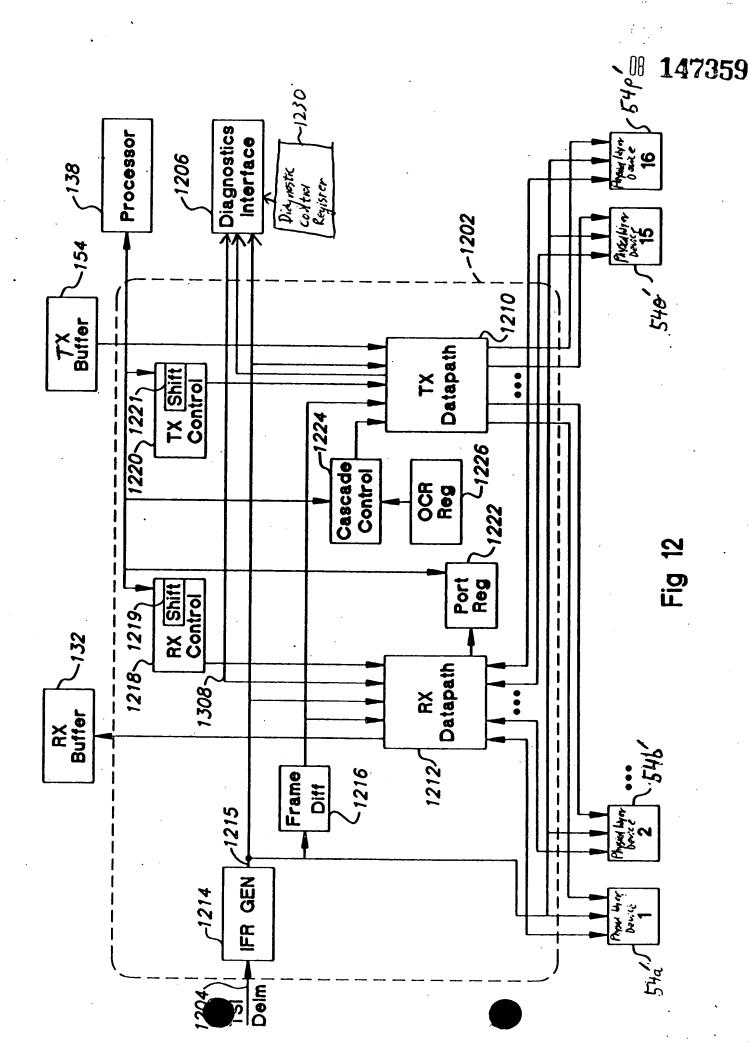


Fig 11



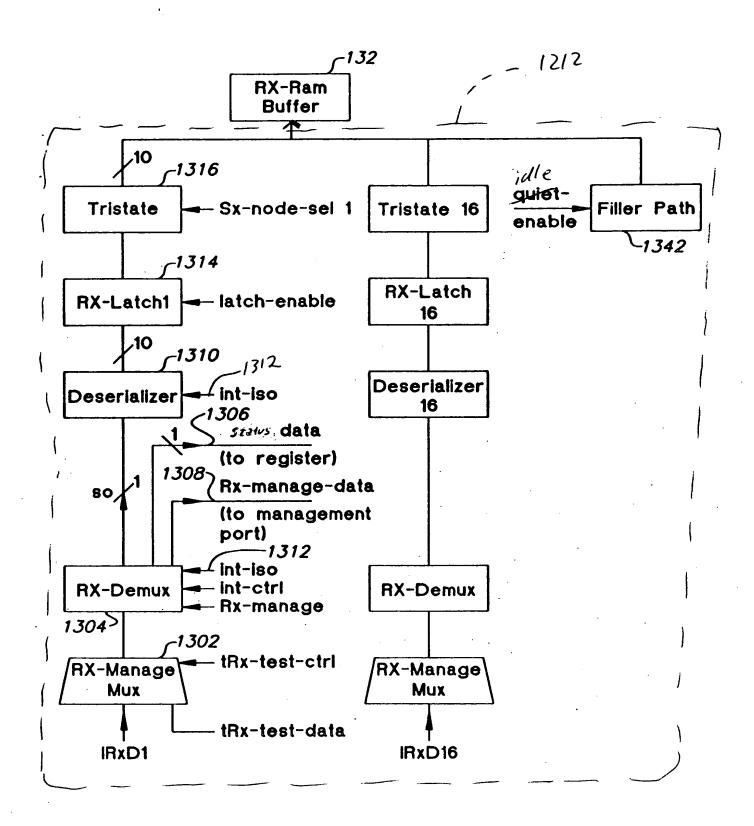
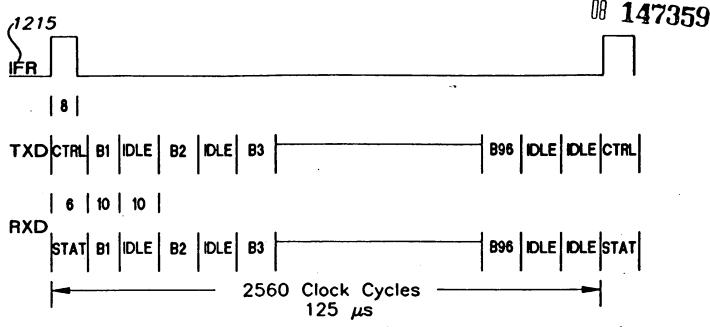


Fig 13

147359 -1210 154 14220 -1422b Quiet Quiet TX-Ram-**Buffer** Pattern 1 Pattern 2 1428 ETE-I 1424 ZIPE tx-RAM-Muxl 1426 10 10 1416 -1416a 1444 - tx-node-sel 1 Tx-Latch 16 Tx-Latch 1 1432 **CAS-Address** Cascade CAS-Rw--1434 **FIFO** CAS-enable 10 Cascade 10 -1602 -1410 - Load-enable Serializer Serializer 1412: 1418 1406-Cidle-data Control Dataint-isoz 1412 6-mux int-idle tr-mux int-ctrl 1402 ITxD16 ITxD1

Fig 14



TXD: Data sent from Isochronous Data Exchanger to Physical

Layer Portion.

RXD: Data Received by Isochronous Data Exchanger from

Physical Layer Portion

IFR: Isochronous Frame Sync signal sent from Isochronous

Data Exchanger to Physical Layer Portion.

CTRL: Control data sent from Isochronous Data Exchanger

to Physical Layer Portion.

STAT: Status data sent from Physical Layer Portion to

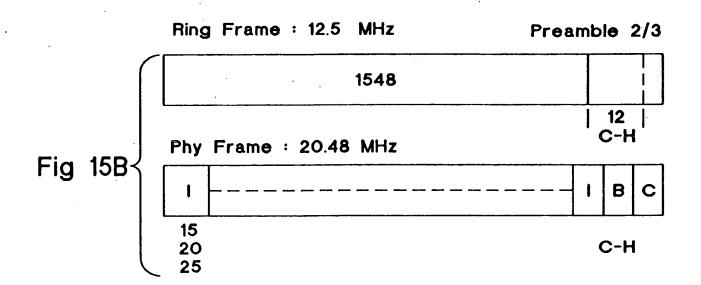
Isochronous Data Exchanger.

B(1:96): B channel data (96 bytes of Bchannel data per

 μ s cycle).

IDLE: Filler data.

Fig 15A



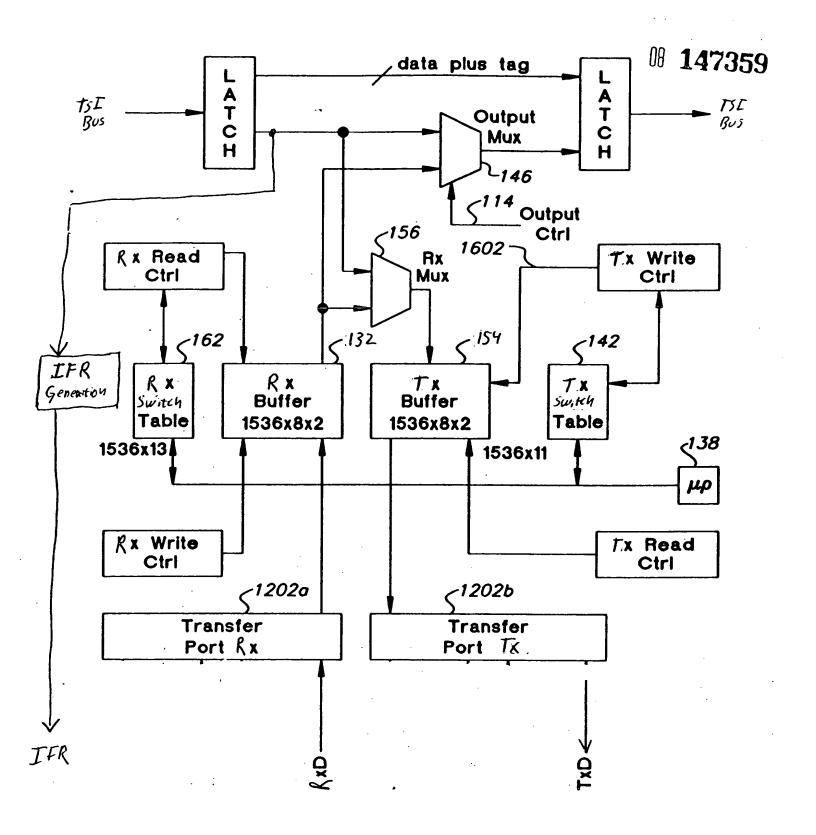
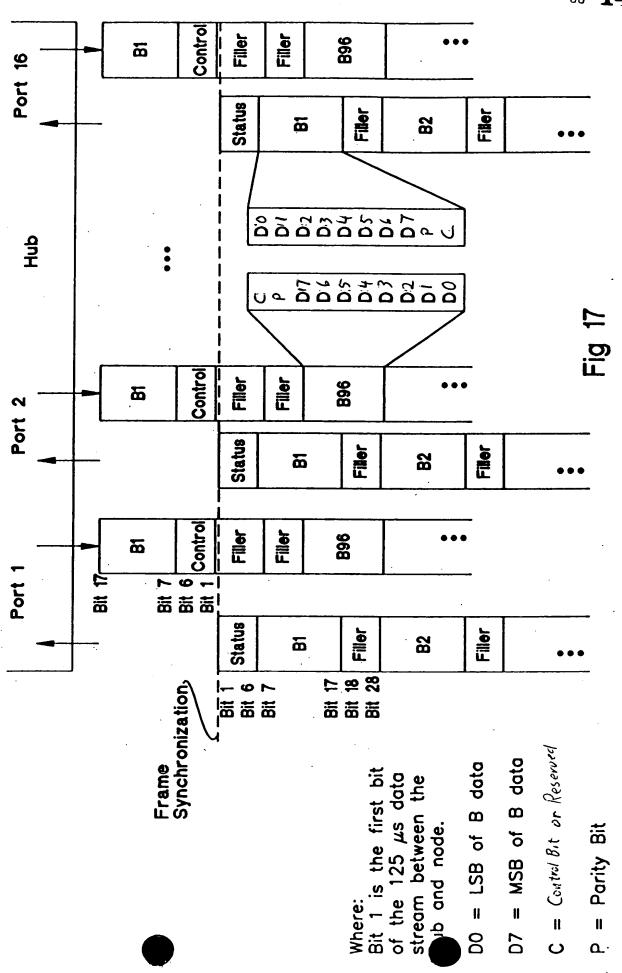


Fig 16



まら	CV2	P A
	۷٦	906
	M9J	A.
	4AD	Date
	DINT	80
	INId	Stat
		P
Bit 🧏	SBR	mitt
Bit £	S38 BES	ansmitt
Bit £	020	Transmitt
Bit &	SES	Jata Transmitt
) Bit ¹	BES BES	ol Data Transmitt
Bit 0 Bit 2	HES HES HES	Control Data Transmitt

Control Bits

RES: Reserved bit.

Status Bits

Coscade bit: Used to activate the port 1 cascade logic. CAS:

Link Active: Indicates that the link is isochronous active when set

Low Power Mode: Indicates theat the isophy is in low power mode when set.

LPX:

₹

S.

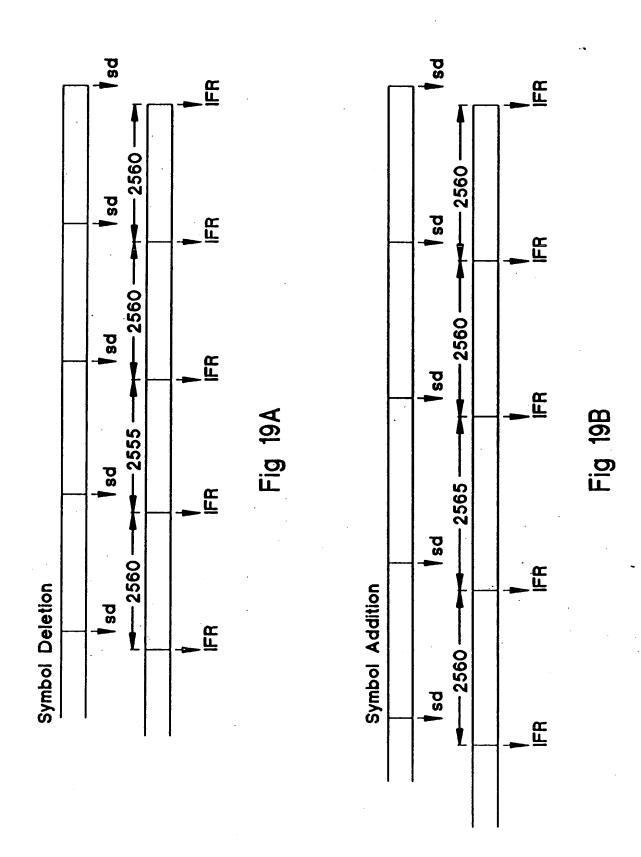
CAPacity: Indicates the type of Isochronous capacity. "1" 15.872 Mbps Isochronous bandwidth "0" 6,144 Mbps Isochronous bandwidth D INTerrupt: Indicates that the isophy has received a start of D channel packet when set.

M INterrupt: Indicates that the isophy's maintenance has changed when set.

PIN T:

DIN T

Fig 18



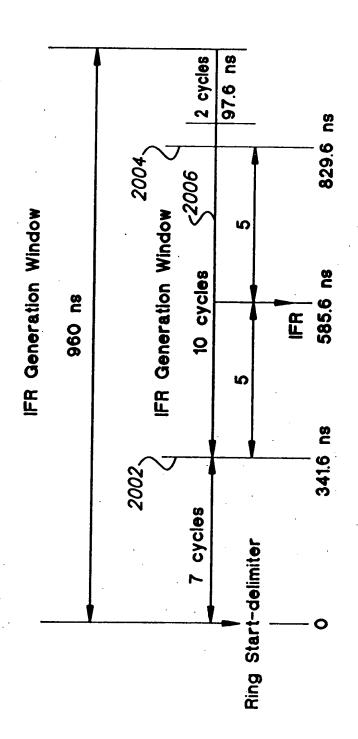
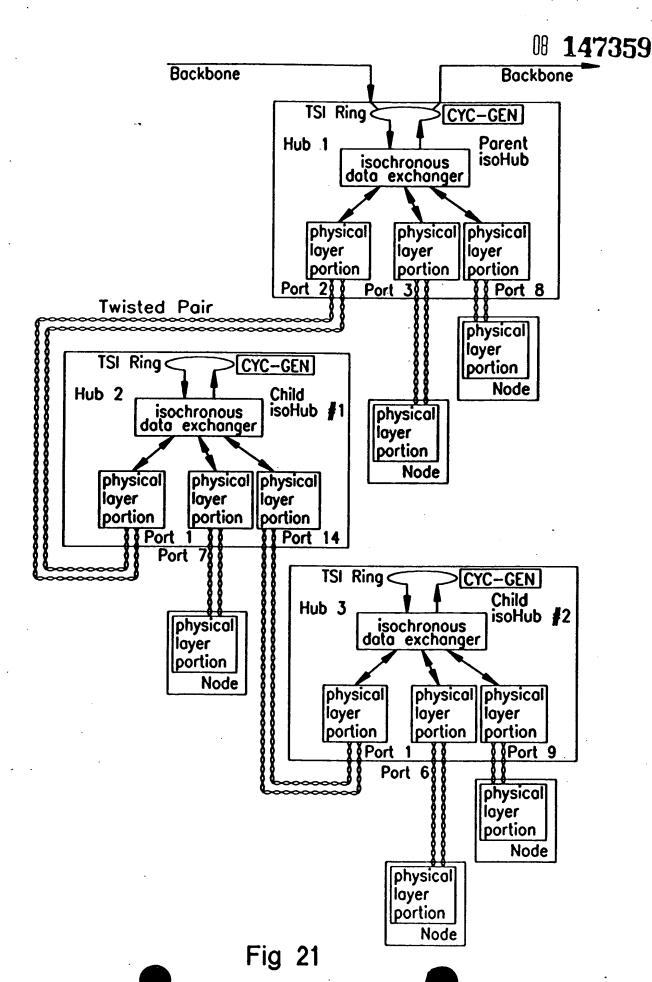
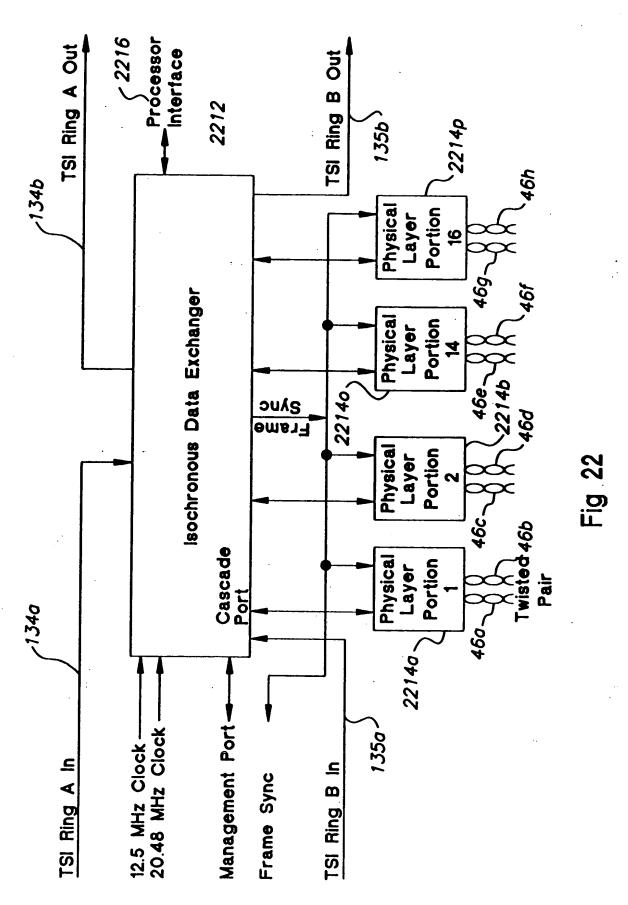
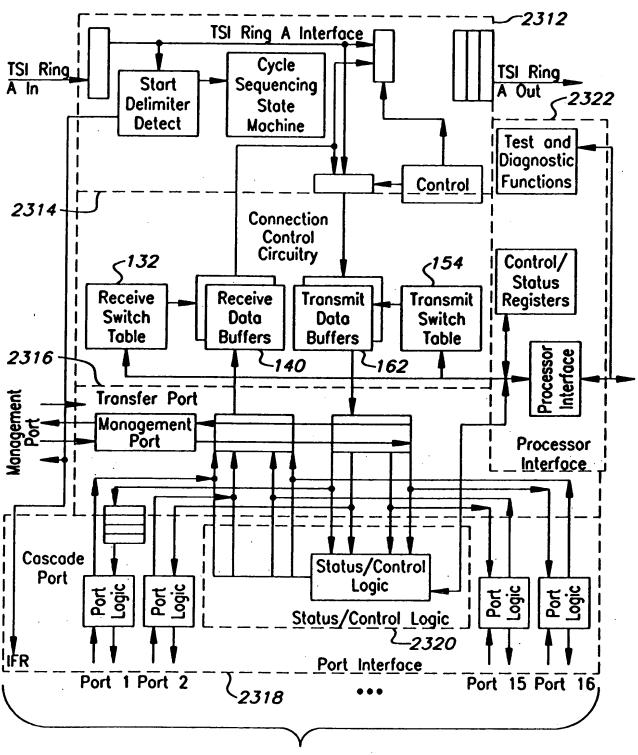


Fig 20





Mode 1 TSI Ring A To Isochronous Physical Layer Interface



To Isochronous Physical Layer

Mode 2 TSI Ring A To TSI Ring B

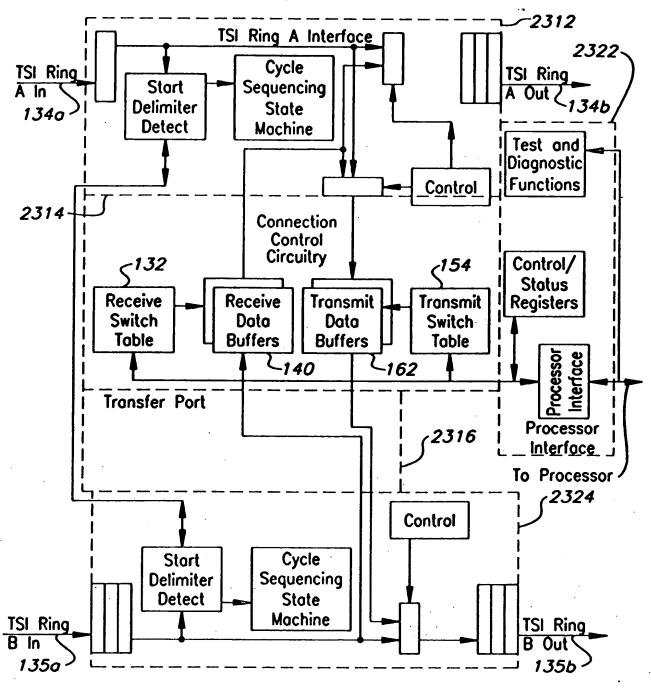


Fig 23B

Data Buffer Address

Switch Table Address	R	eceiv	e Sw	itch '	Table	
Isochronous Maintenance Channel (IMC)	0	Parity	TȘE	ITE	ETE	Data Buffer Address
TSI Ring A Slot 1	1					
TSI Ring A Slot 2	2					
•	•					•
TSI Ring A Slot 1535	1535					
TSI Ring A Slot 1536	1536					
		MSB 1 Bit	1 Bit	1 Bit	1 Bit	LSB LSB
		Fig	3 24	HA		

Switch Toble Address

Not Used

			Usea		<u> </u>	<u> </u>	
Port 1, B channel 1	1						
Port 2, B channel 1	2						
•						•	
Port 14, B channel 96	1535						;
Port 2, B channel 96	1536						
		MSB 1 Bit	1 Bit	1 Bit	1 Bit	11 Bits -	LSB

Transmit Switch Table

Fig 24B

Bit Definitions

IA: Idle Address:

Indicates the idle pattern to be sent.

ITE: Internal Transmit Enable: Indicates an Internal loopback of the slot when set.

IPE: Idle Pottern Eg

Indicates the use of a qu pattern when set.

Réceive Switch Table Switch Table Address Isochronous Maintenance **Parity** 0 TSE Data Buffer Address ITE ETE Channel (IMC) TSI Ring A Slot 1 TSI Ring A Slot 2 2 TSI Ring A Slot 1535 1535 TSI Ring A Slot 1536 1536 **MSB** LSB 1 Bit 1 Bit 1 Bit 1 Bit -– 11 Bits -Fig 25A

Transmit Switch Table

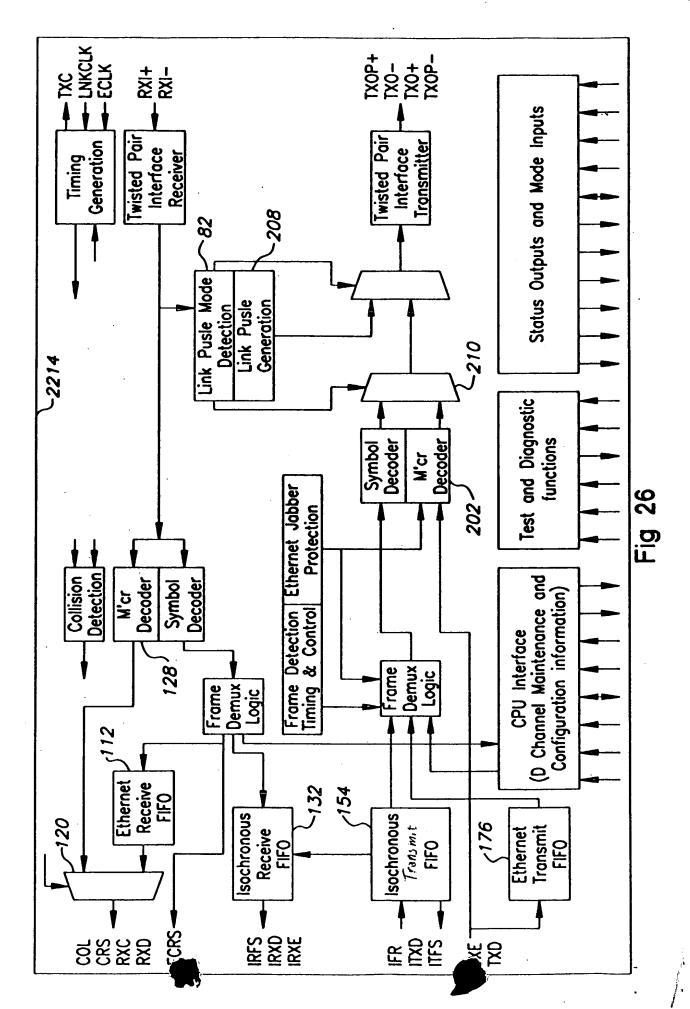
Switch Table Address						
Isochronous Maintenance Channel (IMC)	0	Parity	TSE	Not Used	ETE	Data Buffer Address
TSI Ring B Slot 1	1					
TSI Ring B Slot 2	2					
•						•
TSI Ring B Slot 1535	1535					
TSI Ring B Slot 1536	1536					
		MSB 1 Bit	1 Bit	1 Bit	1 Bit	LSE
		F	ig 2	5B		

Bit Definitions

ETE: External Transmit Enable: In Mode 2, indicates an External switching of slot when set.

TSE: Tri-State Enab.

The isoTSX drives the TStating output drivers when set.



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